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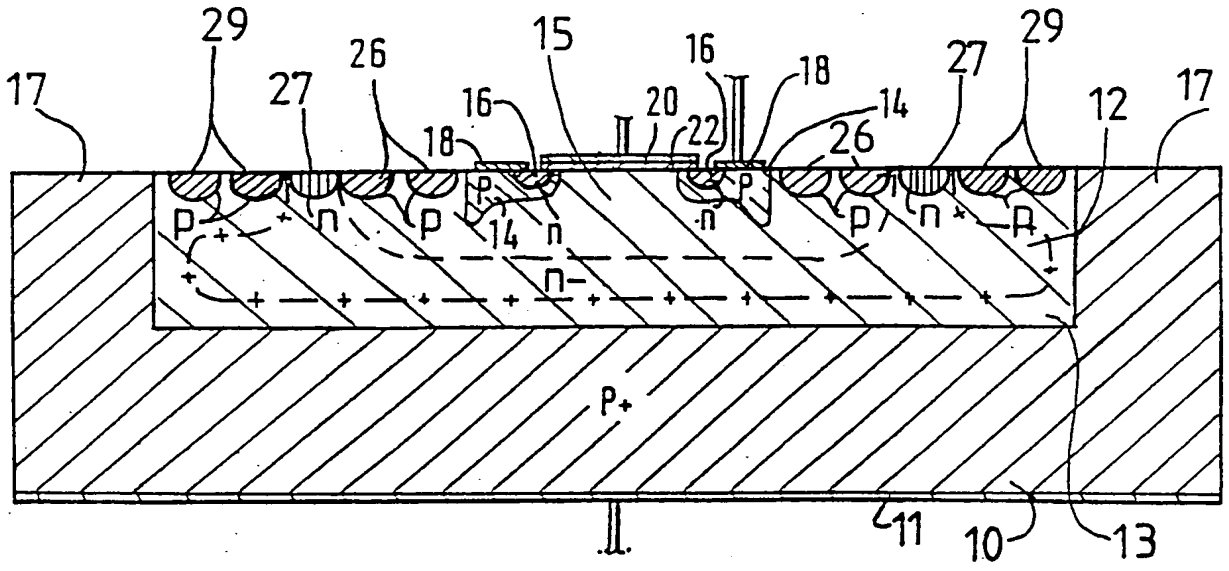

(57) Abstract

An insulated gate bipolar transistor comprises four regions of alternate conductivity type semiconductor material between anode and cathode electrodes (11, 18). An insulated gate electrode (20) establishes current flow from the cathode (18) into a base region (12) adjacent the anode region (10). The anode region (10) has a portion (17) which is brought to the surface on which the cathode electrode (18) is disposed. High voltage field rings (26, 27, 29) are formed in the surface of the base region (12) between the anode and cathode regions (17, 14), the field rings serving to maintain the width of the depletion layers (13, 15) of the anode-base and cathode-base PN junctions.

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Insulated gate bipolar transistor

This invention relates to a semiconductor device and more particularly to a power switching device in the form of an insulated gate bipolar transistor with an improved reverse breakdown voltage rating.

An insulated gate bipolar transistor comprises four layers or regions of alternate conductivity-type semiconductor material disposed between an anode electrode and a cathode electrode. A gate electrode is positioned adjacent the cathode electrode but is insulated from the body of semiconductor material. The two intermediate regions extend to the surface of the semiconductor body underneath the insulated gate and the intermediate layer closer to this surface extends to the cathode electrode. When an appropriate potential is applied to the gate electrode, the electric field which is created serves to drive away majority carriers from and attract minority carriers to a nearby zone of that intermediate region thus creating an inversion channel through which charge carriers can pass between the adjacent regions. The device is thus switched on and current flows between the anode and cathode electrodes.

The voltage at which the device breaks down is given as the integral of the built-in electric field (prevailing when the transistor is at equilibrium) across the width of the depletion layer at the PN junction which is reverse biased. If the depletion layer is narrow, the device breaks down at a low voltage. At the edge of the device the depletion layer becomes narrower, causing the voltage rating to fall.

Insulated gate bipolar transistors are known that have a high voltage rating when the anode is positive with respect to the cathode, due to the provision of field rings adjacent the normally reverse-biased cathode-base PN junction, these field rings keeping the depletion layer wide at the edge of the device.

These insulated gate bipolar transistors have a poor voltage breakdown rating however, when the cathode is positive with respect to the anode, due to the reverse-biased anode-base PN junction having a narrow depletion layer at the edge

of the device. This depletion layer is situated at the junction of the semiconductor substrate and the alternate conductivity type epitaxial layer and is therefore buried deep in the device. If field rings are to be used to make the depletion layer wider at the edge of this junction, they have to be diffused from the under surface of the device, which is both complicated and costly.

We have now devised an insulated gate bipolar transistor which overcomes these problems to provide a device with an improved reverse voltage rating without requiring the patterning of the under surface of the device.

In accordance with this invention, there is provided an insulated gate bipolar transistor comprising a body of semiconductor material having four layers of alternate conductivity type disposed between opposite surfaces of the body, anode and cathode electrodes on respective ones of the opposite surfaces, and an insulated gate for establishing charge carrier flow to a base region of the device adjacent the anode region, wherein the anode region extends to the surface on which the cathode electrode is disposed.

Preferably one or more high voltage field rings are formed in the base region between the anode and cathode regions.

The base region is preferably encircled by an annulus of alternate conductivity type semiconductor material which forms part of the anode region.

The base region is preferably lightly doped so the depletion layers of both anode-base and cathode-base junctions spread into this region.

Both anode-base and cathode-base junctions are terminated on the upper surface of the device and preferably the width of their depletion layers are controlled by separate field control rings for each junction.

In another embodiment the same field rings may control both anode-base and cathode-base junction depletion layers.

Embodiments of this invention will now be described by way of examples only and with reference to the accompanying drawings, in which:

FIGURE 1 is a diagrammatic section through a prior art insulated gate bipolar transistor;

FIGURE 2 is an equivalent circuit diagram of the device of Figure 1;

FIGURE 3 is a diagrammatic section through an embodiment of insulated gate bipolar transistor in accordance with this invention; and

FIGURE 4 is a diagrammatic section through another embodiment of insulated gate bipolar transistor in accordance with this invention.

Referring to Figure 1, there is shown a prior art silicon insulated gate bipolar transistor 30 which comprises a p+ substrate or anode region 10, on which a relatively thin epitaxial n- base layer 12 is grown. An anode electrode 11 is applied to the lower surface of the device, i.e. the outer surface of the anode region 10. An annular p region 14 is formed in the base layer 12 at the top surface of the device by diffusion and an annular n+ region 16 is formed in the region 14 at the top surface by ion implantation or by diffusion. An annular cathode electrode 18 is applied to the top surface of the device over the junction between the regions 14 and 16. A gate electrode 20 is applied to the top surface of the device but is insulated therefrom by an insulating layer 22, so as to cover the central zone of the base region 12 and to extend over the narrow annulus of the p region 14 between the central zone of the base region 12 and the n region 16. An annular n type region 27 is formed in the upper surface of the base region 12 to form a field control ring. Two annular p type field control rings 26 are formed between the outer n type field control ring 27 and the p type cathode region 14 in the upper surface of the base region 12.

Figure 2 shows the equivalent circuit of the insulated gate bipolar transistor 30 of Figure 1 when connected as a switch for load L. The device 30 can be considered to comprise a PNP type bipolar transistor T configured in common collector mode and a P-channel MOSFET M. When the gate 20 is appropriately biased, the MOSFET M provides a low resistance path between the base 12 of the bipolar transistor and the negative supply -V rapidly switching the integral PNP bipolar transistor T into

conduction, allowing current to flow through the load L. The MOSFET M has a very high resistance on turn off, which causes the anode-base junction 10, 12 to cease conduction and thereby halt current flow through the load L.

In normal use of the device shown in Figure 1 therefore, a potential is applied to the anode electrode 11 which is more positive than the potential applied to the cathode electrode 18, and then a positive potential can be applied to the gate electrode 20 to turn the device on. In particular the electric field created around the gate electrode drives majority charge carriers (holes) away from and attracts minority charge carriers (electrons) into the narrow annulus of the p region 14 between the central zone of the base 12 and the n region 16, so as to create an inversion channel through this narrow annulus. Carriers then flow along this channel from the n region 16 to the base, with the effect of forward biasing the anode-base junction 10, 12 allowing the majority carriers (holes) in the anode region 10 to be injected across the junction into the base region 12 to become minority carriers therein. The depth of the base is small enough to prevent these minority carriers (holes) recombining with the majority carriers (electrons), thus most of the minority carriers (holes) will reach the reverse biased cathode-base junction 14, 12. Because this junction is reverse biased it only conducts minority carriers (holes), hence these minority carriers (holes) in the n- base region 12 pass through to the cathode 18, completing the flow of current between anode 11 and cathode 18.

The reverse biased cathode-base junction 14, 12 has a depletion layer 15 which mainly spreads into the lightly doped n- base region 12, and is extended widthwise by the two p type field control rings 26 adjacent the cathode 14. The n type field control ring 27 forces the termination of the depletion layer 15 at the top surface between the outer p type and n type field control rings 26, 27. Thus the depletion layer 15 is kept wide at the top surface of the device, to maintain a high forward operating voltage. In order to turn the device off the potential is removed from the gate electrode 20 and the inversion channel disappears in the annular p region 14, preventing flow of charge

carriers into the base region 12.

Under certain conditions the anode 11 may become negative with respect to the cathode 18 due to voltage transients caused by motors or other reactive loads to which the device is connected. Alternatively the device may be incorrectly inserted or a fault may occur in the external circuitry, in any case the device could be damaged if it was subjected to a voltage exceeding the reverse bias voltage rating of the anode-base PN junction 10, 12. In conventional insulated gate bipolar transistors this voltage rating is low compared with its voltage rating under normal operating conditions, due to the narrowing of the anode-base PN junction depletion layer 13 at the edges of the device.

In accordance with this invention and referring to Figure 3, the depletion layer 13 is kept wide at the edges of the device, whilst avoiding the need for field rings formed from the under surface of the device. The device shown in Figure 3 is basically similar to the device shown in Figure 1 and like parts are given like reference numerals. The device is formed from an initial p+ type substrate 10 to form the anode region on which an epitaxial n- base layer 12 is grown. An annular p+ region 17 is diffused down through the layer 12 to reach the p+ type substrate 10, so that the anode region is extended to the upper surface around the base region 12. The outer p type annular field control rings 29 are added between the anode-base junction 10, 12 and the n type field control ring 27 at the upper surface of the base region 12.

When the device of Figure 3 is connected in the manner shown in Figure 2, its operation will normally be the same as for the device of Figure 1. However if the anode 11 becomes negative with respect to the cathode 18, the reverse biased anode-base 10, 12 will not breakdown at such a low voltage. This is due to the depletion layer 13 being widened at the edge of the PN junction (which is now on the upper surface of the device) by the field control rings 29. Thus the reverse bias breakdown voltage of the device is increased, without the need for complicated and costly patterning of the under surface of the device.

Referring to Figure 4, there is shown another

embodiment of insulated gate bipolar transistor in accordance with this invention. This device is the same as that of Figure 3, except that the annular field control rings 26 and 27 are omitted. The cathode-base depletion layer 15 under device forward bias is terminated at the upper surface of the device between the outer field ring 29 and the portion 17 of the anode region, whilst the anode-base depletion layer 13 under device reverse bias is terminated at the upper surface of the device between the inner field ring 29 and the cathode region 14.

Whilst the devices which have been described have a p type substrate, they may instead have an n type substrate (in which case all other regions would be of opposite conductivity type from those indicated).

CLAIMS

1) An insulated gate bipolar transistor comprising a body of semiconductor material having four layers of alternate conductivity type disposed between opposite surfaces of the body, anode and cathode electrodes on respective ones of the opposite surfaces, and an insulated gate for establishing charge carrier flow to a base region of the device adjacent the anode region, wherein the anode region extends to the surface on which the cathode electrode is disposed.

2) An insulated gate bipolar transistor as claimed in claim 1 in which one or more high voltage rings are formed in said base region between the anode and cathode regions.

3) An insulated gate bipolar transistor as claimed in claim 2 in which said field rings are formed on the surface on which the cathode electrode is disposed.

4) An insulated gate bipolar transistor as claimed in any preceding claim in which said base region is lightly doped so that depletion layers of both cathode-base and anode-base junctions spread into said base region.

5) An insulated gate bipolar transistor as claimed in any preceding claim in which the cathode-base and anode-base junctions are terminated on said surface on which the cathode electrode is disposed.

6) An insulated gate bipolar transistor as claimed in any preceding claim, comprising separate field control rings arranged to control the width of anode-base and cathode-base depletion layers.

7) An insulated gate bipolar transistor as claimed in any one of claims 1 to 5, comprising one or more control rings arranged to control the width of both anode-base and cathode-base

junction depletion layers.

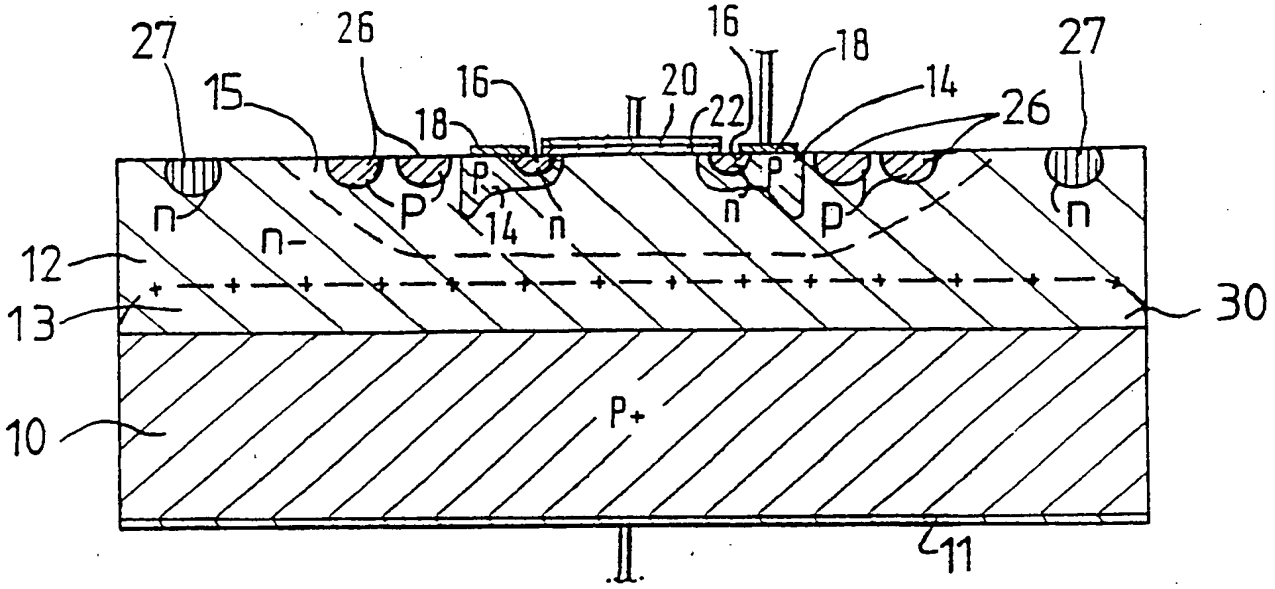

FIG.1

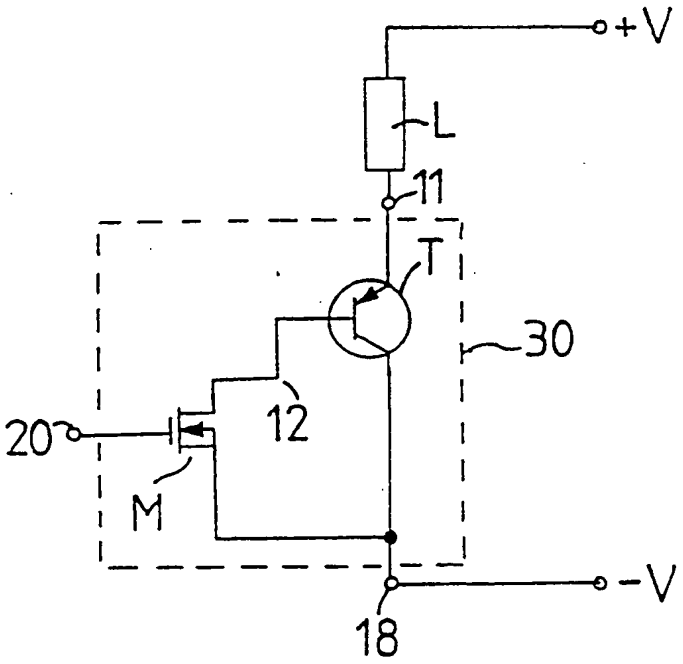

FIG. 2

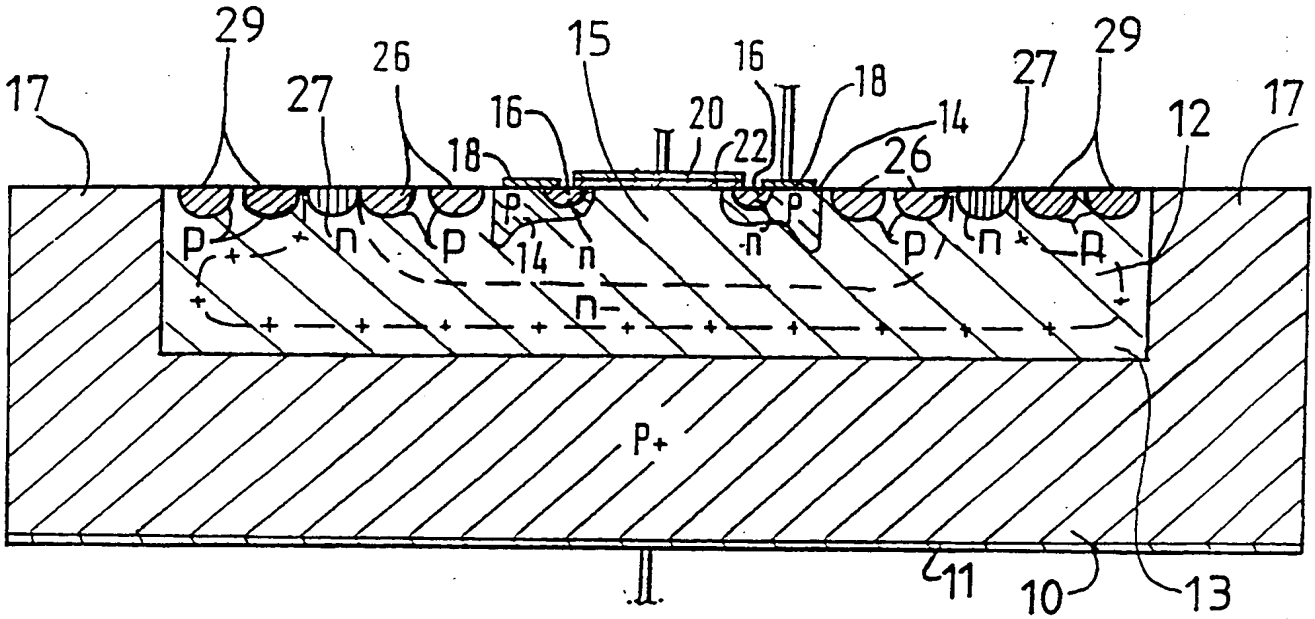

FIG. 3

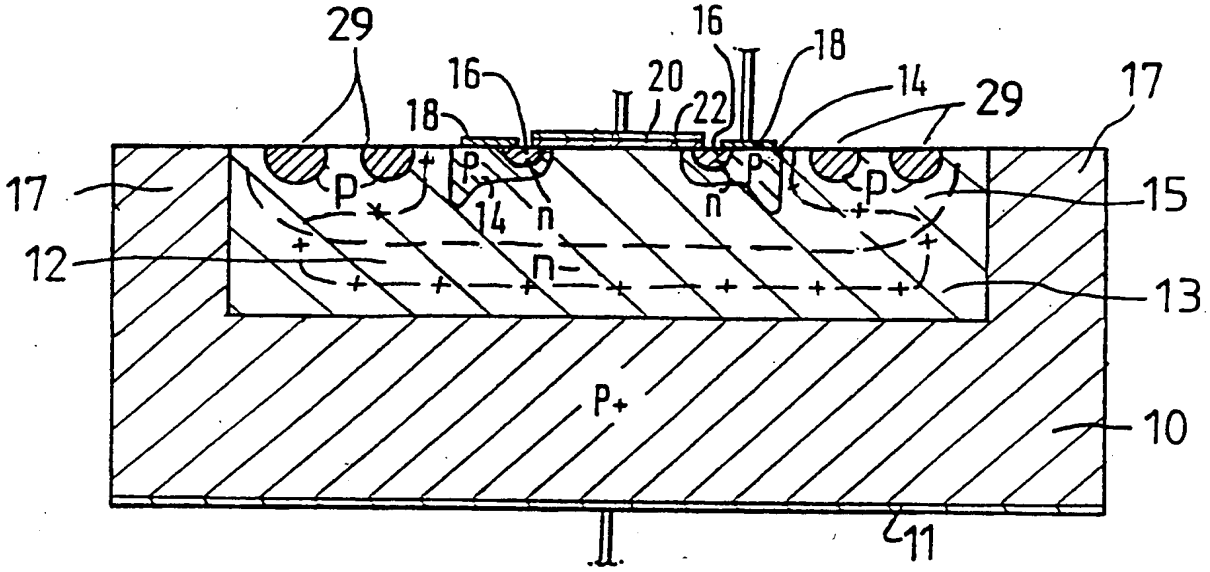

FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 91/00673

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: H 01 L 29/72, H 01 L 29/08

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[5]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	Patent Abstracts of Japan, vol. 14, no. 205 (E-921)(4148), 26 April 1990, & JP, A, 02044776 (FUJI ELECTRIC CO LTD) 14 February 1990 see the abstract; figure 1	1,4
Y	--	2,3,5-7
Y	US, A, 3391287 (KAO et al.) 2 July 1968 see column 4, lines 38-53; figure 5	2,3,6,7
	--	
Y	EP, A, 0332955 (SIEMENS AG) 20 September 1989 see page 3, column 4, line 51 - page 4, column 5, line 4; figure 1	5
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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
6th August 1991	13. 09. 91
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A	Patent Abstracts of Japan, vol. 29, no. 31 (E-475)(2478), 29 January 1987, & JP, A, 61198781 (TOSHIBA CORP.) see the abstract; figure 1	1-3

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. GB 9100673 SA 47118

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3391287		GB-A- 1138237	
EP-A- 0332955	20-09-89	JP-A- 1274471	02-11-89

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